Case #: 12 **Examiner's Name:** Bataille

Serial Number: 09/591,615 **Program Part:** Full

Home SPE: Kim **Art Unit:** 2186

Evaluation Summary: Clear Error(s)

Indicated PEF Clear Errors:

- ☐ 1a compliance with formal requirements
- ☐ 1b technological accuracy
- ☑ 2 treating disclosure statements and claims of priority
- ☐ 3 planning field of search
- ☑ 4 conducting search
- ☑ 5 analyzing disclosure and claims for compliance with 35 USC 112
- ☑ 6 formulating rejections under 35 USC 102 and 103 with supporting rationale, or determining how claim(s) distinguish over the prior art
- ☑ 7 determining whether amendment introduces new matter
- ☐ 8 determining whether restriction is proper
- ☐ 9 determining whether claimed invention is operable/useful as disclosed
- ☐ 10 evaluating/applying case law as necessary
- ☐ 11 evaluating sufficiency of affidavits/declarations
- ☐ 12 determing whether appropriate line of patentable distinction is maintained between application and/or patents
- ☐ 13 evaluating sufficiency of reissue oath/declaration
- ☐ 14 evaluating appropriateness of ground of reexamination

PEF Details:

Improper treatment of priority claim -- no certified copy found in the file.

Claims 3, 4, 5, "first requestor" and "second requestor" lack antecedent basis. They are circuits.

Claim 12 does not make sense. There is no previously recited step of selecting results.

Page 9 of the final rejection, the 103 statement should be Pawate et al. in view of Boutaud et al. based upon the constructions of the rejection which followed.

For the 102 rejection, "teaching" is generally a term for an obviousness type rejection for the references used to modify the primary reference. Since the 102 standard is of inherency, it is more correct to say the reference "discloses". A minor point but sometimes the attorneys argue the examiner has not made a proper 102 rejection if key terms are not present.

No indication on file wrapper that the examiner attempted to review the related applications which are incorporated by reference on page 1 of the spec.

Neither the attorney or the examiner does a great job of addressing Claim 8's rejection. Both arguments appear to be more specific than (or even at odds with) the claim language.

On pages 9 and 11, US patents are cited, but the examiner has not informed the applicant that they have not been considered (see FP 6.49.06).

The incorporation by reference on page 11 is improper. Both US patents discussed there contain

incorporations to other applications in their respective specifications which prevents the applicant from making them the basis for an incorporation by reference. The public should not have to do unlimited construction of references in order to determine how to make or use the applicant's device.

Claim 11 appears to introduce new matter: "the sum of the first portion and the second portion." The spec discusses the first and second portions being of different sizes. Then on page 7, line 24+, the shared memory portion 42b has a size S3 that is equal to S1 minus S2, but that is not the same as saying the sum of the first and second portions equals the total size. The total size of the memory is usually a preset value that is carved into subportions. Making the portions additive theoretically could result in overruns in that allocation (I.e., not enough memory for the applications/circuits being used).

Indicated AT Clear Errors:

- ☑ **a includes all reasonable rejections and/or objections, (MPEP 707.07(g)**
- ☐ **b makes no unreasonable rejection**
- ☐ **c makes no unreasonable formal requirement**
- ☐ **d takes no arbitrary or capricious action**
- ☐ **e makes the record, taken as a whole, reasonably clear and complete**
- ☑ **f properly treats all matters of substance in applicant's response**

AT Details:

Claims 3, 4, 5, "first requestor" and "second requestor" lack antecedent basis. They are circuits.

Claim 12 does not make sense. There is no previously recited step of selecting results.

Claim 11 appears to introduce new matter: "the sum of the first portion and the second portion." The spec discusses the first and second portions being of different sizes. Then on page 7, line 24+, the shared memory portion 42b has a size S3 that is equal to S1 minus S2, but that is not the same as saying the sum of the first and second portions equals the total size. The total size of the memory is usually a preset value that is carved into subportions. Making the portions additive theoretically could result in overruns in that allocation (I.e., not enough memory for the applications/circuits being used).

The response to applicant's arguments regarding Claim 8 is unclear. The examiner does not appear to adequately address the argument the "control registers are not shared" and the claim recites the sharing occurs in the first mode of operation.

The incorporation by reference on page 11 is improper. Both US patents discussed there contain incorporations to other applications in their respective specifications which prevents the applicant from making them the basis for an incorporation by reference. The public should not have to do unlimited construction of references in order to determine how to make or use the applicant's device.

Indicated Allowability Clear Errors:

- ☐ **a determines that all claims are patentable (under 35 USC 102 and 103), over the art of record**
- ☐ **b determines that all claims are patentable (under 35 USC 102 and 103), over all art which is not of record but should have been**
- ☐ **c determines that all claims are patentable over all other pertinent sections of the statue (e.g., 101, 112, 251, etc.)**
- ☐ **d determines that all claims are patentable over all non-statutory rejections (e.g., obviousness type double patenting)**

Allowability Details:

NONE

Monday, September 15, 2003 10:29:21 AM